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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

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07/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,606	DHONG ET AL.	
	Examiner	Art Unit	
	CHAT C. DO	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-8,10-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8,11-13 and 15-19* is/are rejected.

7)☒ Claim(s) *10 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 05/14/2008.

2. Claims 1, 3, 5-8, 10-13 and 15-20 are pending in this application. Claims 1 and 13 are independent claims. In Amendment, claims 2, 4, 9 and 14 are cancelled. This Office Action is made non-final after a RCE filed 05/14/2008.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5, 11-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elliott et al. (U.S. 5,880,983) in view of Gerwig et al. (U.S. 2004/0122886).

Re claim 1, Elliott et al. disclose in Figures 2 a floating point execution unit (e.g. Figure 2) for performing multiply/add operations (e.g. abstract and col. 3 lines 39-46) using a plurality of operands taken from an instruction having a plurality of operand positions (e.g. corresponding to A, B, and C operands as mentioned in col. 1 lines 21-50), wherein the performing does not implement operand formatting selection and unpacking, thereby increasing a speed at which the floating point number is output, the floating point unit (e.g. Figure 2) comprising: a multiplier (e.g. component 102 in Figure 2B) for calculating a product of two of the operands (e.g. as output of multiplier 102 with A and

C as input operands in Figure 2B); an aligner (e.g. components first and second aligners 118 in Figures 2A and 2B) coupled to the multiplier for aligning said product and a third of the operands in a first data path (e.g. third operand is B as seen in Figure 2A); wherein the first data path for supplying to the multiplier operands from a first and a second of the operand positions of the instruction (e.g. first data path for feeding A and C operands into multiplier 102 in Figure 2B); a second data path for supplying the third operand to the aligner (e.g. data path for feeding B into muxes 114 and 116 in Figure 2A); and a multiplexer (e.g. muxes 114 and 116 in Figure 2A) on the second data path for selecting, for use by the aligner, either the operand from the second operand position of the instruction (e.g. operand A) or the operand from the third operand position of the instruction, thereby increasing a speed at which the floating point number is output (e.g. operand B as seen in Figure 2A).

Elliott et al. fail to disclose the aligner is directly couple to the multiplier. However, Gerwig et al. disclose an architecture of a multiplication having an aligner is directly couple to the multiplier (e.g. aligner 10 in Figures 1-2).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to have the result of multiplier couple directly to the aligner as seen in Gerwig et al.'s invention into Elliott et al.'s invention because it would enable to enhance the system performance by directly aligning (e.g. paragraphs [0011-0012]).

Re claim 3, Elliott et al. further disclose in Figures 2 aligner includes means to compute a shift amount for aligning said product and the third operand (e.g. components

111 and 118 in Figure 2A); and the multiplexer operates to select the third operand in parallel with the means to compute the shift amount (e.g. components 114 or 116 in Figure 2A).

Re claim 5, Elliott et al. further disclose in Figures 2 each of the operands and said product includes an exponent value (e.g. as part of floating point number system as seen in col. 1 lines 21-57), and the means to compute computes said shift amount based only on said exponent values (e.g. inherently as for adding correctly as seen in Figure 2A).

Re claim 11, Elliott et al. further disclose in Figures 2 the means to compute the shift amount compresses two of the three input exponents and an offset while selecting the third exponent (e.g. two of three inputs exponents are belong to addends as seen in Figure 2A).

Re claim 12, Elliott et al. further disclose in Figures 2 when executing an add or subtract instruction, the means to compute the shift amount computes the alignment shift amount as ea+eb-2eb (e.g. Figure 2A as difference between the adding operand in order to align properly).

Re claim 13, it is a method claim having similar limitations cited in claim 1. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 15, it is a method claim having similar limitations cited in claim 3. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 16, Elliott et al. further disclose in Figures 2 the multiplexer selects the third operand while the aligner computes the shift amount (e.g. Figures 2A-2B).

Re claim 17, it is a method claim having similar limitations cited in claim 5. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

5. Claims 6-8 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elliott et al. (U.S. 5,880,983) in view of Gerwig et al. (U.S. 2004/0122886), as applied to claims 1 and 13, and in further view of Willson Jr. et al. (U.S. 7,228,325).

Re claims 6-8, Elliott et al. in view of Gerwig et al. fail to disclose in Figures 2 each of the operands has an exponent value, and floating point execution unit determines whether the exponent values of any of the operands is zero in parallel with operation of the multiplier and the aligner; floating point execution unit tests the exponent values for a zero value while the multiplier calculates the product; the floating point execution unit establishes a test result number based on results of the determination.

However, Willson Jr. et al. disclose each of the operands has an exponent value, and floating point execution unit determines whether the exponent values of any of the operands is zero in parallel with operation of the multiplier and the aligner (e.g. col. 7 line 60 to col. 8 line 15); floating point execution unit tests the exponent values for a zero value while the multiplier calculates the product; the floating point execution unit establishes a test result number based on results of the determination (e.g. as for bypass the adder and claims 30-31).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add each of the operands has an exponent value, and floating point execution unit determines whether the exponent values of any of the operands is zero in parallel with operation of the multiplier and the aligner; floating point execution unit tests the exponent values for a zero value while the multiplier calculates the product; the floating point execution unit establishes a test result number based on results of the determination as generally seen in concept in willson Jr. et al.'s invention into Elliott et al. in view of Gerwig et al.'s invention because it would lower power consumption (e.g. col. 7 lines 50-65 due to bypassing the adder/multiplication computation).

Re claim 18, it is a method claim having similar limitations cited in claim 6. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 19, it is a method claim having similar limitations cited in claim 7. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Allowable Subject Matter

6. Claims 10 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 3, 5-8, 11-13 and 15-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

July 21, 2008

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/821,606	DHONG ET AL.	
	Examiner	Art Unit	
	CHAT C. DO	2193	